AMENDMENTS TO THE SPECIFICATION:

Please amend page 2, lines 29-30 as follows:

An object of the present invention is to provide a nonvolatile semiconductor memory device in which data can be electrically erased and can be easily written at a low voltage.

Please amend page 3, line 11 as follows:

According to the nonvolatile semiconductor memory device of the present invention, since the impurity diffused control region is formed at the main surface of the semiconductor substrate to control a potential of the floating gate, a large potential difference can easily be provided between the substrate and the floating gate and thus electrons are easily drawn from the floating gate. Consequently, electrical erasure can be made.

Please amend page 25, lines 10-11 as follows:

ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory device includes: a semiconductor substrate having a main surface; a pair of p-type impurity diffused regions, formed at the main surface of the semiconductor substrate to serve as source/drain; a floating gate formed on a region of the semiconductor substrate lying between the paired p-type impurity diffused regions, with a tunnel

insulating layer interposed between the floating gate and the region of the semiconductor substrate; and an impurity diffused control region formed at the main surface of the semiconductor substrate to control a potential of the floating gate. Accordingly, a nonvolatile semiconductor memory device can be obtained in which data can be electrically erased and written at a low voltage.

Please amend page 13, line 21 as follows:

In write and erase operations, when a voltage as shown in tables 3 and 4 is applied to n-type well region 2a and one source/drain impurity diffused region 11 (or the other source/drain impurity diffused region 11), a depletion layer is formed at pn junctions between n-type well region 2a and p-type semiconductor substrate 1 and between one source/drain impurity diffused region 11 (or the other source/drain impurity diffused region 11) and the ~~p-type region~~ p-type well 12. As the depletion layer extends further, leakage current associated with the punch-through increases.

Please amend page 14, line 17 as follows:

In write and erase operations, when a voltage as shown in tables 3 and 4 is applied to n-type well 2a and one source/drain impurity diffused region 11 (or the other source/drain impurity diffused region 11), a depletion layer is formed at pn junctions between n-type well region 2a and p-type semiconductor substrate 1 and between one source/drain impurity diffused region 11 (or the other source/drain impurity diffused region 11) and the ~~p-type region~~ p-type well region 12.

As the depletion layer extends further, leakage current associated with the punch-through increases.

Please amend page 21, lines 19-20 and line 30 as follows:

P-type well region 32 is formed at the main surface of semiconductor substrate 1. In p-type well region 32 is formed impurity diffused control region (n-type impurity diffused region) 31. ~~P-type well region 12~~ P-type well region 32 has higher carrier concentration than semiconductor substrate 1.

Please amend page 21, line 30 as follows:

In write and erase operations, when a voltages as shown in tables 7 and 8 is applied to n-type well region 2a and impurity diffused control region (n-type impurity diffused region) 31, a depletion layer is formed at pn junctions between n-type well region 2a and p-type semiconductor substrate 1 and between impurity diffused control region (n-type impurity diffused region) 31 and the ~~p-type region~~ p-type well region 32. As the depletion layer extends further, leakage current associated with the punch-through increases.

Please amend page 12, line 13 as follows:

In this case, a negative voltages as shown in table 4 is also applied to the pair of p-type impurity diffused regions 3, 3 to lower the floating gate 5 potential (with reference to one p-type impurity diffused region 3). To perform an efficient erase operation, a junction capacitance ratio of floating gate 5 to one source/drain impurity diffused region 11 (or the other source/drain

~~impurity diffused region 3~~ impurity diffused region 11) is preferably minimized to obtain a maximum potential difference.

Please amend page 19, Table 7 as follows:

(Table 7)

REGION WHERE VOLTAGE IS TO BE APPLIED	VOLTAGE
ONE P-TYPE IMPURITY DIFFUSED REGION 3	0V
THE OTHER P-TYPE IMPURITY DIFFUSED REGION 3	~8V
IMPURITY DIFFUSED CONTROL REGION 31	~5V
N-TYPE WELL REGION 2a	~8V
P-TYPE SEMICONDUCTOR ~~SUBSTRATE 31~~ [[SUBSTRATE 1]]	0V

*Same voltage is applied to the other p-type impurity diffused region 3 and n-type well region 2a.

Please amend page 20, Table 8 as follows:

(Table 8)

REGION WHERE VOLTAGE IS TO BE APPLIED	VOLTAGE
ONE P-TYPE IMPURITY DIFFUSED REGION 3	~ -10V
THE OTHER P-TYPE IMPURITY DIFFUSED REGION 3	~ -10V
IMPURITY DIFFUSED CONTROL REGION 31	~15V
N-TYPE WELL REGION 2a	0V
P-TYPE SEMICONDUCTOR ~~SUBSTRATE 31~~ [[SUBSTRATE 1]]	0V

*Same voltage is applied to one p-type impurity diffused region 3 and the other p-type impurity diffused region 3.

Please amend page 20, line 19 as follows:

In this case, a negative voltage as shown in ~~table 6~~ table 8 is also applied to the pair of p-type impurity diffused regions 3, 3 to lower the floating gate 5 potential (with reference to one p-type impurity diffused region 3). To perform an efficient erase operation, junction capacitance ratios of floating gate 5 to one p-type impurity diffused region 3, the other p-type impurity diffused region 3, and n-type well region 2a respectively are preferably minimized to obtain a maximum potential difference.